Chip back potential is the level which bulk silicon is maintained by on-chip connection, or it is the level to which the chip back must be connected when specifically stated below. If no potential is given the chip back should be isolated.

**PAD FUNCTIONS:**

1. **1A**
2. **1Y**
3. **2A**
4. **2Y**
5. **3A**
6. **3Y**
7. **GND**
8. **4Y**
9. **4A**
10. **5Y**
11. **5A**
12. **6Y**
13. **6A**
14. **VCC**

**.057”**

**12 11 10 9**

**2 3 4 5**

**13**

**14**

**1**

**8**

**7**

**6**

**MASK**

**REF**

**.055”**

**Top Material: Al**

**Backside Material: Si**

**Bond Pad Size: .005 X .005”**

**Backside Potential: GND**

**Mask Ref:**

**APPROVED BY: DK DIE SIZE .055” X .057” DATE: 1/26/23**

**MFG: SILICON SUPPLIES THICKNESS .014” P/N: 5407**

**DG 10.1.2**

#### Rev B, 7/1